

Detached Sb-Based Crystal Growth by VDS: Fabrication and Characterization of the Schottky and MOS Devices on InSb VDS-Substrate Operate At 300k

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Abstract: *In this research, Schottky Barrier diode (SBD) and MOS structure fabrication process on substrates (n-InSb, p-InSb) from the detached crystals grown by the vertical directional solidification (VDS) have been reported. An interface layer between the Al/n-InSb SBD, and Al/Oxide/n-InSb MOS-structure had been fabricated and studied. For Sb-based devices - leakage current, generation recombination (g-r), Shockley-Read-Hall (SRH), and series resistance (Rs) are analyzed. The performance of VDS-devices has drastically influenced by the quality of interface, deposited metal (Al) on n-InSb VDS substrate, and the dielectric layer (oxide) between (Al) and substrate (n-InSb). InSb VDS-substrate status, SBD and MOS parameters are characterized at 300K. The ideality factor (η) decreases to near unity, while series resistance lowers with increase in InSb crystal quality, it reveals increased barrier height (BH). experiments of device characteristics have been performed at 300K by the C-V, Rs-V (SBD), I-V, C-V, $G(w)/w-F$, C-F (MOS) methods, and also comparison of VDS-device and traditional-device are discussed.*

Keywords: *Solidification, Interface layer, Sb-based crystal growth, Fermi level, Dielectric properties, Oxidation, Eelectronic materials, Eelectrical and electronic characterisation*

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I. Introduction

Antimonide (Sb-based) III-V materials have the potential in third generation infrared devices (IR) and integrated circuit (IC) for a high speed, low power and high breakdown voltage. In addition, these devices have significance in space exploration, biomedical spectroscopy, military systems, THz amplifiers and high speed complementary logic circuits [1]. Moreover, Sb-based electronic devices for example - high speed heterojunction bipolar transistors (HBTs), High electron mobility transistors (HEMTs) from InSb/AlSb and high hole mobility InGaSb/AlSb quantum well heterostructure field effect transistors (HFETs) have opened a new novel research area. As well, Sb-based heterostructures (AlSb, InSb, GaSb, InGaSb, GaAsSb and InGaAsSb) employed in high speed, and low power applications. An added uses are wide-bandwidth telecommunications for aircraft, satellites, wireless communication, global positioning systems, thermo-photovoltaic cells, and THz medical imaging and remote sensing [2]. The mono-crystalline InSb/GaSb substrates in the epitaxial deposition demand a large size and the ultra high quality crystals for IR and optoelectronic devices for high yield [3]. Aim of space grown materials were to study the buoyancy driven convection, the ultra high quality achieved by the suppression of thermo-gravitational convection in a melt, it could lead to the increased crystal quality [4]. A comprehensive survey of the detached crystal growth in outer orbital space shuttles showed improved physical properties of crystals [5]. The fabrication of the metal-semiconductor (M-S) interface for SBD an important technology [6,7] has effects on the electrical and optical properties [8]. This technology used in the electronics industry in microelectronics, solar cell, chemical sensing, and radiation detector for the x-rays γ -rays. For the Metal-Oxide-semiconductor (MOS) technology, the lack of a compatible oxide a supreme challenge to replace silicon with Sb-based III-V materials have tremendous ongoing search for suitable dielectric to unpin the Fermi level. Recent devices become more complex to use silicon oxide (SiO₂) because of highest leakage current and higher power consumption. The C-V frequency dispersion plot related to the defects in interfacial layer for the high mobility and high-k dielectric [9]. The basic parameter and the dark current mechanism is necessary for fundamental study (viz. I-V, C-V, C-F, Rs-V) [10]. The traditional InSb-substrate limitation: i) at high temperature (300K) hindered operation, ii) InSb detector performance stuck mainly by the large leakage current, iii) a radiation detector need development of the high-quality InSb crystals, iv) the systematic studies of fabrication process needed for devices performance. In view of these prime problems, we had achieved solidification of the Sb-based bulk crystal (InSb, GaSb and doped materials) under controlled growth condition

and parameters for device grade substrates, and published elsewhere [11,12]. The entire detached Sb-based crystals have grown by VDS (InSb and GaSb bulk crystals) of high quality and defects free. This occurrence is analogous to the crystal grown in outer orbital spacecraft [11]. Spatial uniformity of the Sb-based mono-crystalline substrates [12] would fulfill fabrication requirements of the manufactures, and showed the highest physical properties for the crystals grown ever. For the first time, Sb-based detached crystal (VDS-substrates) [13] were used for the fabrication of SBD, MOS for investigating the leakage current at 300K. A analysis of suppression or elimination of the adverse factors will be proposed [14]. No report for leakage current of VDS-substrates have been cited. However, recent advanced high-mobility / high-k technology of the Sb-based substrates (III-V) proposed as the enhanced electric properties. The VDS-devices performance by I-V, C-V, Rs-V at 300K have been reported, and also examined to compare with existing devices. In this report quality affecting parameters - native defect, recombination, $g-r$, SRH, R_s , density of interface traps (D_{it}), number of surface state (N_{ss}) are also discussed.

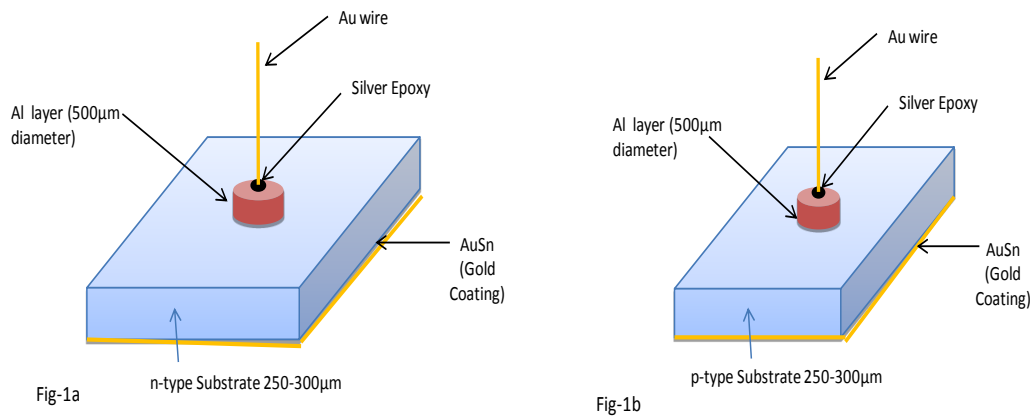


Figure 1. Schematic Schottky diode (SBD) fabrication process on - a) n-type and b) p-type InSb VDS-substrates

II. Experimental Procedure

II.1 Sb-based substrates from the detached crystals

For the first time Sb-based substrates grown by VDS used for the fabricating Schottky diode with Al-metallization, and MOS structure by anodic oxidation on InSb at 300K are presented. These InSb substrates specification are - i) Substrates: complex type InSb (p-type up to $\sim 125K$, n-type it above); ii) Dimensions: mirror polished $10 \times 10 \times 0.3 \text{mm}^3$; iii) Preferential growth direction: (220); iv) Mobility (μ): $6.05 \times 10^4 \text{cm}^2/\text{V}\cdot\text{sec}$; v) Carrier concentration: $n \sim 3.8 \times 10^{16} \text{cm}^{-3}$; vi) Energy bandgap: $E_g \sim 0.16 \text{eV}$; vii) Resistivity: $3.0 \times 10^{-3} \Omega\text{-cm}$; viii) Cut-off wavelength: $\lambda \sim 7.3 \mu\text{m}$; ix) Each pit density: $\text{EPD} \leq 10^3 \text{cm}^{-2}$; x) FWHM: $\sim 65 \text{arcsec}$; xi) Micro-Hardness: $H_v \sim 2.2 \text{GPa}$.

II.2 InSb VDS-Schottky diode fabrication

The polished, cleaned wafers of undoped InSb and Te doped n-InSb (220) were used for fabrication of Al/n-InSb and Al/p-InSb interface for SBD. The substrates were kept into methanol before loading to prevent oxidation. A mask of $500 \mu\text{m}$ diameter was used for preparation of Aluminum (Al) patterns. The ohmic contacts Al on the substrates were done in a vacuum (10^{-5} torr) by thermal evaporation method. The metallization was carried at 200°C for one minute in flowing hydrogen, so that Al contact dots forms on the InSb substrates. VDS-SBD is shown in Fig-1a for p-InSb, and n-InSb in Fig-1b. Measurements of I-V, C-V and R_s -V plots were made at 300K.

II.3 InSb VDS-MOS device fabrication

The fabrication of InSb VDS-MOS, n-type and p-type InSb wafers were polished one side and other side was lapped. For an anodic oxidation process, non-aqueous electrolyte was prepared by 10gms of Ammonia pentaborate in 100cc of ethylene glycol. The PH of the solution was adjusted by the adding NH_4OH and tartaric acid. The oxidation layer was formed by a constant current density ($13.5 \text{mA}/\text{cm}^2$) by an oxide growth rate $40 \text{A}/\text{V}$ up to the formation voltage 100V . The array of Al dots of $500 \mu\text{m}$ diameter were deposited on the oxide layer through the shadow mask in vacuum (10^{-5} torr) evaporation. InSb VDS-MOS structure is shown in Fig-2a for n-type and Fig-2b for p-type VDS-substrates, then used for characterization. The measurements set up for SBD and MOS were Lock-in-Amplifier, SR-530, Keithly 617 programmable Electrometer and 4275 multi-frequency LCR meter from the Research Institute in Mumbai India.

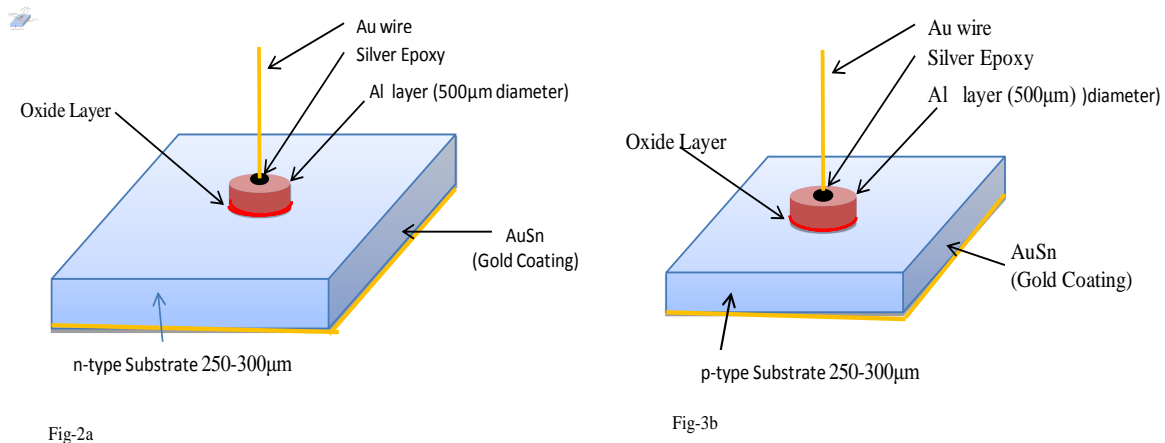


Figure 2. Schematic MOS fabrication process a) p-type and b) n-type on InSb VDS-substrates

III. Results and Discussion

III.1 VDS-InSb Schottky Barrier diode

The brief theory is produced in this paragraph for calculating SBD parameters. The SBD performance and reliability has drastically been influenced by the interface quality between the deposited metal (Al) and InSb substrate surface. No literature cited for VDS-SBD fabrication on the substrates (detached crystals) of the Au/n-InSb and Au/p-InSb interface layer. For the first time, in this investigations the electrical properties of the InSb VDS-SBD at 300K are reported. SBD current carried by the majority carriers dissimilar to a conventional *p-n* junction, and no minority carriers storage effects thus extremely fast switching effect occurs. According to thermionic theory, current expressed by the basic thermionic emission for SBD in Fig.3,4 given by eqn-1 [15].

$$I = AA * T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \left[\exp\left(\frac{q(V-IR_s)}{\eta kT}\right) - 1\right] \quad (1)$$

The saturation current at zero volt is given in eqn-2.

$$I_s = AA * T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \quad (2)$$

Where A: the effective area of InSb VDS-diode (dot $r=250\mu\text{m}$), A^* : effective Richardson constant, theoretically calculated, $A^*=(4\pi k^2 m^*/h^3) = (1.68\text{cm}^{-2}\text{k}^{-2}$ with $m^* = 0.0139m_0$ for *n-type*, $54\text{cm}^{-2}\text{k}^{-2}$ with $m^* = 0.45m_0$ for *p-type*), the A^* is constant at varying temperature; I_s : saturation current, η : ideality factor, V : applied voltage drop across the SBD junction, Φ_b : Schottky barrier height (SBH), T : absolute temperature, q : elementary charge, k : Boltzmann constant, R_s : series resistance, R_{sh} : shunt resistance, R_d : diode resistance,. The current flows through a series combination of R_d , R_s , and R_{sh} .

Forward bias (FB): the rectifying nature of I-V plots indicate the existence of barrier between the ‘Al’ electrode and crystalline n-InSb VDS-substrate as in semi-log I-V and I-V plots at 300K. Fig-3 and Fig-4 (FB) shows the ideal diode curve of rectification, which is comparable to the *p-n* junction diode with the three distinct regions of conduction mechanism. Region-I (0.5-2.5V) linear dependence, the injection from electrode into the n-InSb substrate is reduced for the low bias voltage, and R_{sh} plays significant influence in the semi-log I-V. The I-V curve shows the effect of parasitic resistances, a linear response at low positive and negative biases, whereas current

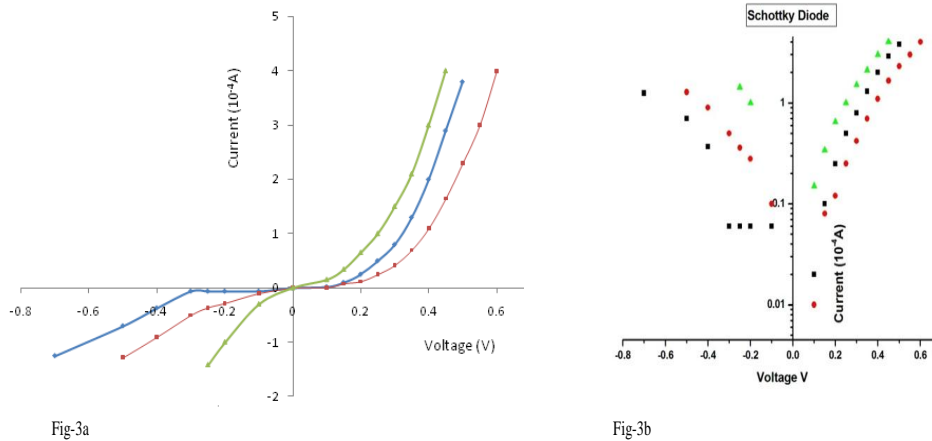


Figure 3. the Schottky barrier diode (SBD), a) I-V and b) semi log I-V characteristics of difference regions n-InSb substrate-1 at the 300K, and Regions: I- linear (0.5-2.5V), II- $I \sim \exp V$ (0.3 to 0.4.5V), III- $I \sim V^2$ (> 0.5V)

controlled by R_{sh} . Region-II (0.3 to 0.4.5V) exponentially increase ($I \sim \exp V$), an exponential response at middle bias portion of curve is used to know n and I_s where current controlled by the diode Eqn-1, 2, while dominant transport mechanism is recombination (g-r, SRH). In semi-log I-V Fig-3, and 4 the lower curvature of the I-V plot (knee) shows the effect of interface parameters (η , R_s , R_{sh}). The ' η ' values from these regions near to unity for SBD, viz. Red (R) $\eta = 1.09$, Blue (B) $\eta = 1.17$, Yellowish (Y) $\eta = 1.28$ (R-B-Y), it showed rectifying property on the InSb VDS-substrate on smooth surface. For low quality substrates η increases with decrease in SBH, where the larger ' η ' related to the presence of the g-r, SRH mechanisms. The traps in depletion influenced by R_s , and these mechanisms can be controlled by η and SBH. The presence of an interfacial layer, surface states and defect levels could be the main source for $\eta > 1$ and lower SBH by the carrier recombination. Region-III (> 0.5V) the current in power law ($I \sim V^2$), but R_s plays significant influence on I-V, and Semi-log I-V plots due to the space charge or tunneling current transport mechanism dominant for high bias, and current could be controlled by R_s Fig-3, and 4 (FB). In these regions, a significant reduction in D_{it} relate to increase in SBH for the high crystallinity InSb VDS-substrates. Because of the self-purification and self-passivation during interface growth process, thus interface quality attributed to high order. The R-B-Y-curves (FB) show rectifying nature with slight different from each other for the respective measured cut-in voltages (V_{γ}) or built in voltage (V_{bi}) 0.26V, 0.22V, 0.12V respectively. This voltages reduction from larger to smaller shows strong to weak rectification related to decrease in SBH. The minor rectification variations indicate larger reduction in D_{it} , N_{ss} , and induced dipole mechanism.

Reverse bias (RB): In I-V and Semi-log I-V plots Fig-3, and 4 R-B-Y curves represent the fundamental difference in the interface state, and the metallization process, which were depending on the leakage (dark) current mechanisms at interface - a) g-r, b) SRH, c) defects, d) traps. The I-V (RB) **curves consists of nine points** - i) bulk diffusion by the thermal g-r, ii) surface diffusion along the interface surface, iii) bulk g-r current caused by the traps in the depletion region (shallow states of carriers) and SRH effect, iv) surface g-r current cause by traps on the surface (surface leakages), vi) g-r and shunt current dominant at the low reverse bias, vii) an ohmic (shunt) current in linear I-V caused by metallization process or the surface leakage along edges of interface, viii) the thermal g-r dominant at a high reverse bias, ix) tunneling current generated at high reverse bias by depletion region (traps dominant or deep traps). These **nine points** have been adversely affects the leakages current or breakdown voltage (V_b). These are measured from RB of I-V curves in Fig-3, and 4, and leakages currents are 18 μA , 26 μA , 40 μA linear up to $V_R = 0.65V$, 0.45V, 0.12V for respective curve (R-B-Y). Finally at higher voltage, current generated by heat (thermionic emission eqn-1) by the junction breakdown $V_b > 1V$, 0.7V, 0.2V for respective curve. The higher breakdown voltage for SBD at 300K has been attributed to high quality interface and InSb VDS-substrates. Three cases have been explained for respective curve: **Curve-R**, the rectification with uniform distribution of interface state and increase in SBH, and reasons showed in viii, ix (see **curve consists**). **Curve-B**, the rectifying contact with moderate uniform distribution of interface state and moderate SBH with the reduced defect density, also reasons showed in iii, iv, vi, viii, ix, (see **curve consists**). **Curve-Y**, the weak rectifying contact and non-uniform distribution of interface state with reasons showed in i, ii, viii, (see **curve consists**). On the whole, the Al/InSb interface layer on VDS-SBD has better rectification by fine restructure layer allowing to block indium (In) atoms migration to surface, and excess amount of antimony (Sb) evaporated in the crystal growth (detached) process. Information regarding M-S contacts SBDs were not annealed to avoid thermal defect, and non-uniformity distribution into the interface layer, since annealing was

interrupted the *p-n* junction properties on VDS-substrate [12]. Defects elimination or suppression into crystals (VDS) had attributed to lower leakage (saturation) current, lower ideality factor (η), reduced g-r, SRH, reduced imperfect state in band gap, and tunneling processes. The higher defects densities

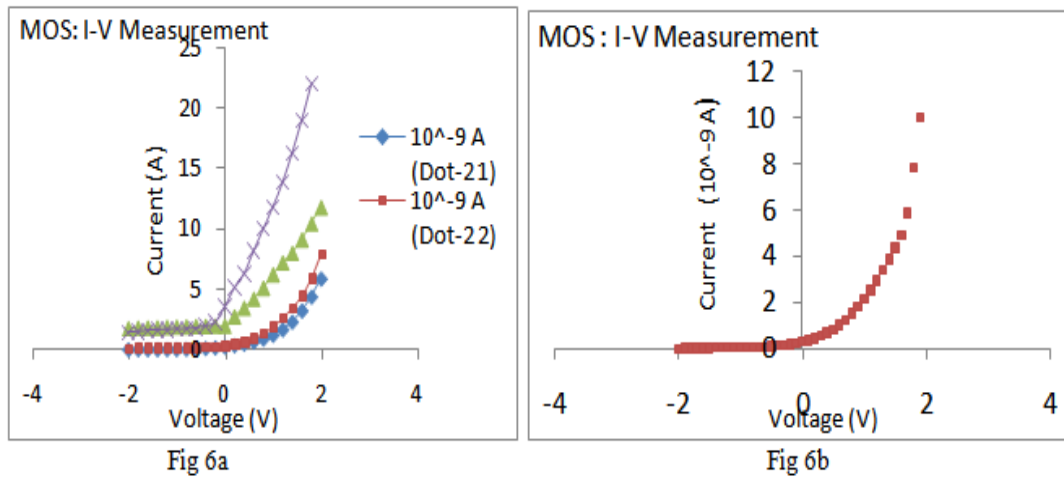


Figure 4. the Schottky barrier diode (SBD), a) I-V and b) semi log I-V characteristics of the different regions *n*-InSb substrate at 300K.

contribute from i) higher reverse leakage current, ii) higher ideality factor and iii) lower barriers height. These are influenced by secondary interface mechanism - interface dipole, induced defects, and fabrication process.

The series resistance (Rs): an ideal case $R_s = \text{zero}$, and $R_{sh} = \text{high}$, but in experimental condition these differs as in Fig-5. For high quality interface, the Al/*n*-InSb SBD showed low series resistance and high shunt resistance. The interface traps and R_s play a significant role on electrical properties. The change in R_s exhibits trap charge has not enough energy [15]. Norde method may be used to determine R_s from eqn-3, as expressed below.

$$R_s = \frac{kT(\gamma - \eta)}{qI} \quad (3)$$

Where γ an integer (dimensionless), $\gamma > \eta$, the values η stated in Region -II, ($R=1.09$, $B=1.17$, $Y=1.28$), and γ is defined as the ratio of the forward current (FB : $R=0.21\mu\text{A}$, $B=0.78\mu\text{A}$, $Y=1.06\mu\text{A}$) to reverse current (RB : $R=-0.075\mu\text{A}$, $B=-0.15\mu\text{A}$, $R=-1.5\mu\text{A}$) at constant voltage, $V=0.25\text{V}$. Thus γ for corresponding ratio (γ : $R=2.8$, $B=5.2$, $Y=7.1$), and the value of $(\gamma - \eta)$ ($R=1.71$, $B=4.03$, $Y=5.82$). R_s calculated on VDS-substrate from different surface regions using these values in Eqn-3. The two cases of R_s measured, **Case FB - I** R_s at 0.25V in Fig-5 (three curves: $R=2.4\text{K}\Omega$, $B=1.3\text{K}\Omega$, $Y=1.2\text{K}\Omega$), similarly **Case RB, II** R_s at 0.25V in Fig-5 (three curves $R=4.7\text{K}\Omega$, $B=1.8\text{K}\Omega$, $Y=1.2\text{K}\Omega$). In this case (I and II) no wide difference, hence junction has rectifying contact with low leakage (dark) or reverse saturation current. The SBD performance in Fig-5 shows lower variation in R_s by superiority of VDS-devices at 300K. While low R_s and high R_{sh} requires to prevent current loss at the interface. The trivial variation in R_s of the Au/*p*-InSb, Au/*n*-InSb SBD interfaces indicate homogeneity in the SBH, which is attributed to low interface traps and superior rectification. The values of R_s decrease with increasing crystal quality. SBD represent series combination of an ideal diode resistor R_D and R_s , through which the current flows, but increase in R_s has influence on I-V deviation from the ideal graph.

The zero bias: Norde method [15] may be used to calculate SBH (Φ_b), eqn-4.

$$\Phi_b = \eta \frac{kT}{q} \ln \left(\frac{AA^*T^2}{I_s} \right) \quad (4)$$

The $\eta=1$ for ideal diode, but InSb VDS-devices η near to unity (1.09, 1.17, 1.28 for R-B-Y), $kT/q = 26\text{mV}$, $T=300\text{K}$, substituting A , A^* and I_s values in Eqn-4 gives correspond Φ_b (0.036eV, 0.033eV, 0.031eV). Φ_b shows the increased SBH by suppression of interface traps, surface states and imperfections. Usually M-S structure with low Φ_b and low SBH are attributed to the presence of interfacial thin layer (traps into barrier), interface traps and native oxide layer. The homogeneity in barrier may deviation from the ideal curve by presence of hazy interface layer, and interface defect accumulation, which depends on quality of M-S interface and metallization.

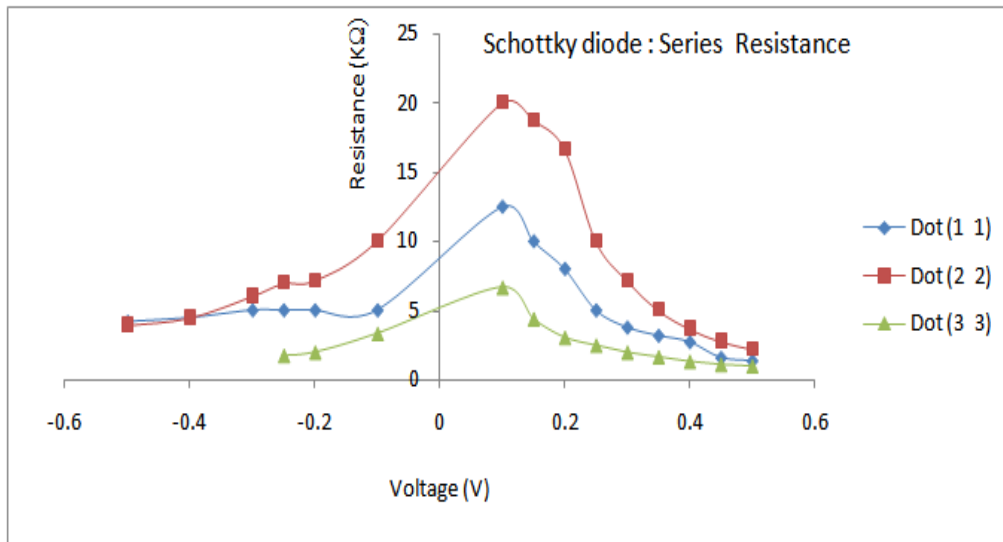


Figure 5. the series resistance R_s Vs applied voltage (V) for Schottky diode at 300K on InSb VDS-substrate

III.2 Metal-Oxide-Semiconductor (MOS) structure

Investigation aim is electrical characterization and parameters study of VDS-MOS device with applied bias voltage at 300K. Recent experiment on high- k capacitors [16] anticipated a leakage current in the range of nA. For an ideal MOS at zero voltage Fermi level $\phi_M - \phi_S = 0$ where ϕ_M work functions of metal and ϕ_S semiconductor, if there is a flat band condition, then D_{it} tends to minimum near flat-band.

InSb VDS-MOS: I-V plot at 300K in Fig-6, this plot shows similarity to an ideal diode in the FB, and a constant low current $< 0.1nA$ in RB, while no current variation owing to high quality VDS-substrates. Four VDS-MOS devices selected from substrate's different region, it reveals an absence of current fluctuation (leakage current) the homogeneous oxide layer by the reduction in interface traps (InSb-Oxide) and the oxide traps in oxide film. The similar nature of graphs implies smooth surface and homogeneous InSb substrates, if an oxide layer with the leakage current ($< nA$). Usually in deposition process, native oxide on surface introduce impurities that facilitate tunnelling of carriers, then influence of a large leakage current need to be eliminated/suppressed. InSb-substrates showed the adequate leakage current, thus the surface oxide layer thickness has been reduced with density of surface state into gap, which decrease the surface band bending. If Leakage current drive out the capacitor charge then it does not function as a capacitor. InSb-samples were used without annealing as explained previously[12], because without annealed InSb VDS-substrates have shown homogeneous dispersion and low leakage current. The n-InSb MOS C-V plots for different frequency (0.5Khz to 1 Mhz) has shown in Fig-7a. The low frequency response (0.5KHz) in Fig-7b shows strong C-V transition (alike Mott-Schottky capacitance) by presence of band bending, similar to the ideal C-V plot. The high quality InSb substrates and interface layer showed no large C-V variation.

The analysis of high-frequency capacitance-voltage (HFCV) for positive voltage in C-V plot Fig-7b is seen with the fast transition from accumulation region to depletion region indicates a relatively low interface trap density between oxide and InSb, similarly the oxide traps into an oxide layer. For negative voltage, the formation of inversion layer corroborates the Fermi level unpinning at interface (Oxide/InSb). Three cases for C-V plot in Fig-7b: (a) Accumulation $V > 0$, (b) Depletion $V < 0$ small negative, and (c) Inversion $V < 0$ high negative. The case (a), first phase of accumulation, the positive bias band bending near n-InSb surface allocate electrons to assemble, thus intrinsic Fermi level dips for accumulation of the additional electrons. The case (b), a small negative voltage,

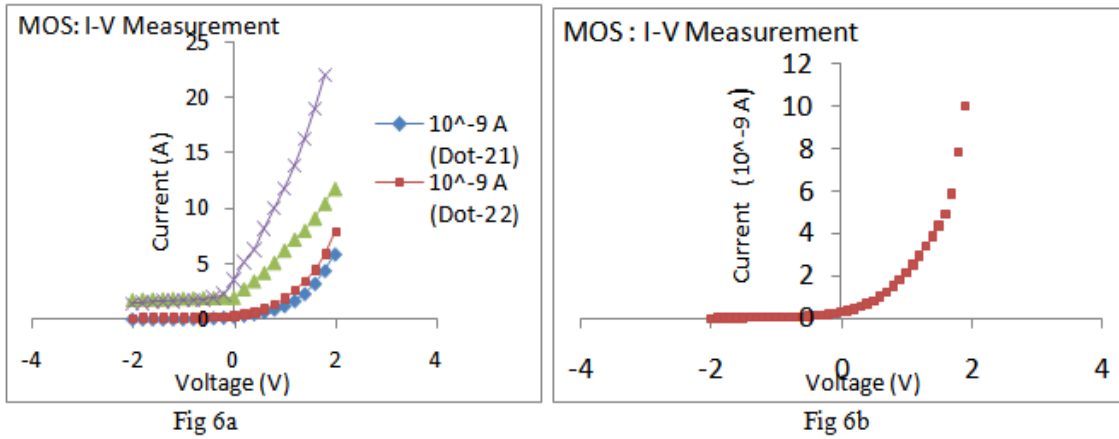


Figure 6. a) MOS I-V characteristics a) on four different region, b) on single region of InSb-VDS substrate at 300K

depletion region is formed by second phase with no charge carriers at the surface but the electrons get away by the negative potential. Further, the depletion region grows with increased negative voltage as the inversion, and form the third phase. The case (c), the sufficient negative potential attracts minority carriers in the n-InSb surface, hence the density of holes lead to a higher concentration with the difference in carriers (hole/Electron) leads increase in upwards band bending, and the fourth phase as the inversion at Cox: oxide capacitance) alike positive bias. The mechanism at low frequency n-InSb MOS at high positive voltage has two cases - i) shows accumulation because of plenty of electrons at the surface go through the oxide as donors, while in ii) true for high negative voltage as acceptors, then the depletion increases as inversion by increases in holes at surface as acceptors, but i) and ii) cases band bending occurs. In low quality InSb substrates, usually capacitors show large variation in recombination process by two type - depending on concentrations and build-up voltages. First type, the carrier recombination in weak inversion, where recombination originate from structural defects at the interface. Second type, deep acceptors operating in the strong surface inversion in which the recombination includes indium vacancy.

A typical basic equations of C-V [19] for the Global Capacitance is given in eqn-5.

$$\frac{1}{C} = \frac{1}{C_{OX}} + \frac{1}{C_{SC}} = \frac{d_{OX}}{\epsilon_{OX} \epsilon_0} + \frac{1}{C_{SC}} \quad (5)$$

Where at 0.5KHz, Cox: oxide capacitance (131pF), Csc: semiconductor capacitance (135pF), d_{ox}: oxide thickness (0.2μ), Global capacitance C (91pF). ε_{ox}: oxide dielectric constant, ε₀: vacuum permittivity. The space charge capacitance denote nearly flat band potential, good for electric properties of an oxide layer. A linear variation of the global capacitance with applied potential shown in Fig-7a, it reveals the presence of an oxide layer. In the inversion of n-InSb, the concentration of holes exceed the electrons as result the inversion layer separated into two process - i) weak- and ii) strong inversion, Fig-7b. In 'weak inversion' no band bending present by lack of difference between the intrinsic and the original metal Fermi level, thus curve shifts in the negative side of voltage -0.2V (128pF), then beyond this voltage band bending result into 'strong inversion' up to 0.5V. As in a low frequency C-V in Fig-7b (0.5KHz) the depletion region g-r of carriers is equal which leads to charge exchange with the inversion layer. The total capacitance reaches Cox (131pF), thus the C-V curve displays an ideal InSb VDS-MOS. In high frequency C-V, the minority carrier response is not seen, but the capacitance stays at the minimum (95pF at MHz). However, the low quality InSb MOS, C-V deviates from an ideal curve associated with rough distribution of impurities especially higher capacitor variation, and leakage current. These are not found in InSb VDS-MOS.

The high frequency capacitance C_{HF} (eqn-6) and low frequency C_{LF} (eqn-7) expressed below -

$$C_{HF} = \left[\left(\frac{C_D - C_{OX}}{C_{OX} + C_D} \right) \right] \quad (6)$$

$$\frac{1}{C_{LF}} = \left[\frac{1}{C_{OX}} + \frac{1}{C_{it} + C_D} \right] \quad (7)$$

Where at 0.5KHz, C_{HF}: high frequency capacitance (97pF at 1MHz), Cox: oxide capacitance (131pF), C_D: depletion layer capacitance (129pF), low frequency capacitance C_{LF} (128pF), interface face traps capacitance (C_{it}: 10¹⁴ pF). A low leakage current (nA) showed by InSb VDS-MOS capacitors, small variation of accumulation capacitance exhibit larger flat-band voltage at different frequencies (0.5Khz-1MHz). The flat-capacitor plateau shows low interface traps by the absence of Sb-rich surface or In-O interfacial layer. Electrical

characteristics signify fabrication process on high quality InSb substrate surface necessary for deposition of oxide layer.

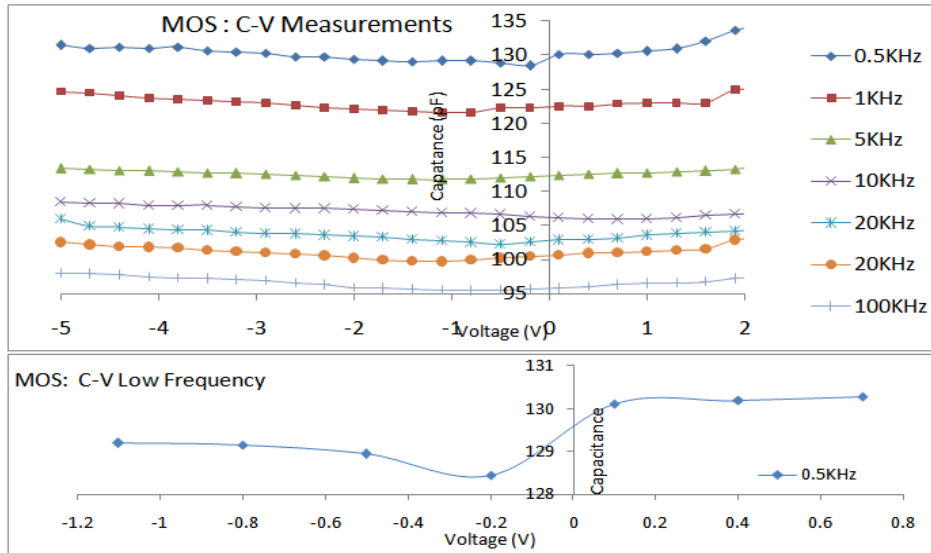


Figure 7 a, b. A typical CV curve at 300K, the high-mobility n-InSb VDS-substrate shows frequency dispersion in accumulation, depletion, and inversion region. A stretch-out location is absent into high-frequency CV curve.

The InSb-MOS Fig-8: C^{-2} -V plot shows nearly flat plateau up to 1.5V, but the capacitance Vs frequency (C-F), and the transconductance Vs frequency ($G(w)/w$ -F) in Fig-8b reveal nearly ideal behavior of the InSb VDS-MOS. The $G(w)/w$ decreases significantly with increase in frequency up to 30KHz, then smoothly increases up to 1MHz, then the capacitance decrease fast at low frequency up to 5KHz. It shows the no significant variation up to 100KHz, then slowly decreases up to 1MHz. These evidences are interpreted by three regions associated with the dissimilar three mechanisms -i) a capacitance excess arises by the electrode polarization (phenomenon) occurrence at low frequencies, while the capacitance is associated with the exponentially enhance with ionic accumulation mechanisms located at the electrode interfaces, ii) experimentally the effect of series resistances R_s reduced the capacitive response at higher frequencies, iii) a constant capacitance plateau developed by the dielectric polarizability of the n-InSb and an oxide material. A central region could be an additional contributions in the depletion layer capacitance, where the central capacitive level only varied marginally. The global capacitance at 0.5KHz high (91pF) constant over a potential range up to 1.5V (eqn-5). The constant capacitances shows the applied

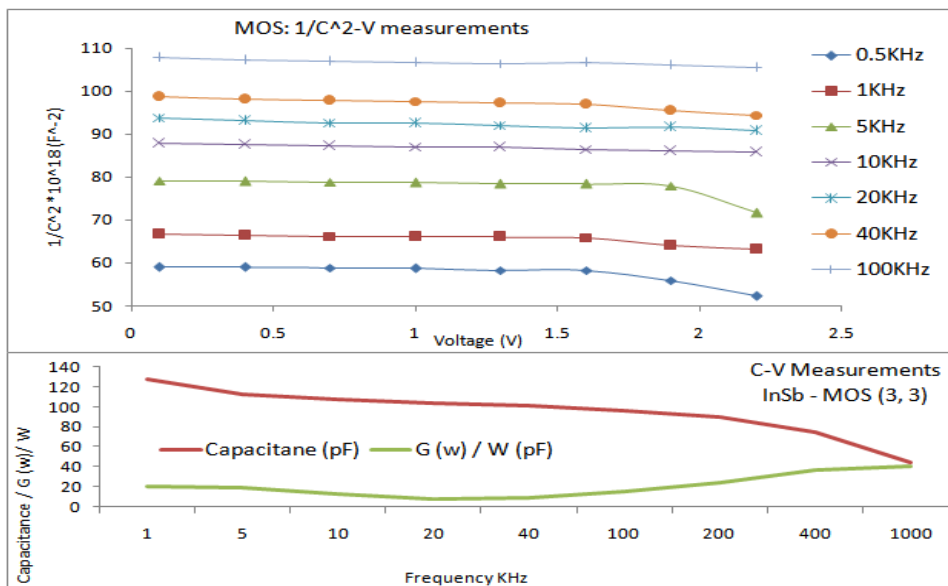


Figure 8 a,b. a) the C^{-2} -V and b) C-F, $G(w)/w$ -F measurements for the n-InSb MOS for zero bias at 300K

potential entirely drop in a homogeneous oxide layer by keeping a constant band bending. The C-V curve steady with negligible variation in capacitance for different frequencies, it is evidence that unlike the shape of the large variation capacitance by the impurity in interface and substrates by the InSb-conventional MOS.

The generation rate 'g' [19] is given by eqn-8

$$g = Gg N_D/C_D \quad (8)$$

Where at 1KHz, the thermally generated conductance $Gg = \sim 10^{-9}$ mhos, depletion capacitance $C_D = 123$ pF, for n-InSb VDS-MOS ($N_D = 2 \times 10^{16} \text{cm}^{-3}$, $C_{ox} = 124$ pF and $C_{min} = 122$ pF) for an oxide dia. $500 \mu\text{m}$. Using these parameters, $g = \sim 1.6 \times 10^{17}$, time constant $T = 10^{-3}$ sec, carrier lifetime (τ). InSb VDS-MOS technology, the low density of interface traps ($D_{it} = \sim 10^9 \text{cm}^{-2} \text{eV}^{-1}$), however, g , T , D_{it} and N_{ss} parameters two order < than cited in literature, may be operate in the charge injection category, it is attributed to enhanced C-V plots by the high quality InSb VDS-substrate. VDS-devices on the InSb substrates have low saturation (dark) current, which establish storage capacity of InSb VDS-MOS capacitor.

The interface capacitance C_{it} is given by eqn-9

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{OX}} \right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{OX}} \right]^{-1} \quad (9)$$

The density of interface traps D_{it} is given by eqn-10

$$\frac{C_{it}}{qA} \quad (10)$$

Where q : electronic charge, A : Area of the device ($r = 250 \mu\text{m}$), $C_{it} = 0.45$ pF, the density of interface traps estimated from Eqn-10, $D_{it} = 10^{10} \text{eV}^{-1} \text{cm}^{-2}$. The C-V characteristics of InSb VDS-MOS is comparable to the high mobility and high- k [21] materials. For investigating the new materials of high-K for leakage current hindrance by SiO_2 , the research is in progress for thermodynamically stable interface from Sb-based (III-V) materials. For instance, Sb-based (III-V) materials with higher carrier mobility, and oxides with higher dielectric constant (k) are under contemplation. Recently tested materials for the high- k (dielectric constant 25) oxides includes Zirconium oxide (ZrO_2), Hafnium oxide (HfO_2) and Titanium oxide (TiO_2) [20], and proposed as the reducing leakage current for ultra-quality devices. Next-generation nonvolatile memory storage could be based on resistive random access memories (RRAMs) in which TiO_2 and HfO_2 used as the resistive switching devices, and characteristics of the unidirectional diode and electronic bipolar switching devices [23]. The irregular C-V in MOS devices with zirconium oxide (ZrO_2) as dielectric has unusual phenomenon, which is not consistent with charge trapping and de-trapping, it is attributed to the interface dipoles at the high- k/SiO_2 interface [24]. To report here is that the InSb MOS fabricated on VDS-substrates had been used without annealing as explained previously [12].

IV. High-Mobility Nibs Substrates from vds

IV.1 InSb SBD on VDS-substrates at 300K

The SBD devices require a low dark current, and this could be achieved from the high quality substrate and fabrication process. In comparison between the InSb VDS and traditional devices: InSb VDS-devices operate at the 300K, on the other hand InSb traditional devices operate at 77K [16], and bariode at 180K [17]. It is reported that the I-V curve of traditional InSb-diodes measured, and its characteristic showed disappearance at 300K [16]. It was attributed - i) no rectification by a large series resistance, ii) a large leakage or dark current, and iii) a large thermal noise. These factors introduce defects into depletion layer by chemical reaction and diffusion. But these diodes showed rectification ≤ 77 K due to reduced leakage current, and at low temperature may be by blocking contacts. On the other hand, VDS-diodes show rectifying at 300K, which is disparity with the traditional InSb diodes, because of enhanced rectifying contact, and high quality of detached crystals. *InSb traditional SBD parameters*: $N_{ss} \sim 10^{14} \text{cm}^{-3}$, $D_{it} \sim 10^{12} \text{eV}^{-1} \text{cm}^{-2}$, effective carrier lifetime $\tau \sim 10^{-9}$ s. *VDS-SBD at 300K*, the *Al/n-InSb interface* parameters (N_{ss} , D_{it}) were estimated, it showed two order < than the InSb traditional-SBD at 77K, and I-V plot showed rectification with drastic reduction in leakage current (μA), η near to unity (ideal diode). Metal deposition on InSb VDS-substrates with highest crystal quality have smooth surface, uniform interface, rectification and low leakage current.

IV.2 InSb MOS structure on VDS-substrates at 300K

InSb traditional MOS parameters: $D_{it} = 10^{11} \text{cm}^{-2} \text{eV}^{-1}$, time constants $T \sim 10^{-5}$ s independent of the bias varies with D_{it} , effective carrier life time $\tau = 10^{-9}$ sec, the mean interface traps capacitance C_{it} , the dielectric constant $\epsilon_s \sim 10^{10} \text{F/cm}$ (InSb/GaSb). InSb VDS-MOS parameters (T , τ) are two order > than the InSb-traditional-MOS. For low quality InSb crystals -i) the distribution of states either fall down on the conduction band side or valence band side, then large density of interface traps pinning the Fermi level, ii) the occupancy of interface defect changes in HFCV by a strong stretch-out, it is attributed to the large concentration of donor-like interface states. Whereas InSb VDS-MOS differ from the former stretch-out concept, because in high quality crystals it was at the high-frequency disappeared may be weak capacitor transition, and showed the ideal C-V curve. InSb-

traditional substrates, frequency dispersion of the accumulation and depletion regions (obscure) show the strong presence of high density of interface state. A large inversion dispersion depends on the interface traps and oxide traps by the minor excess indium formed deep In_2O_3 in acceptor region, and antimony on surface formed Sb_2O_3 in donor side. Besides dissimilarity of InSb VDS-MOS, the interface traps and oxide traps drastically reduced in depletion layer as a result Fermi level unpinned. At the same time, whereas the Sb and In envisaged as the origin of Fermi level pinning. The high- k (III-V) Sb-based interface is complex, reasons- i) density of interface traps is high in the intrinsic Sb-based surfaces, ii) the nature of an oxidation. The electrically active interface defects can be formed during oxidation, Sb-rich regions increases interface traps leads to increase a leakage current. These are responsible for dispersion in the depletion layer. The interface traps and non-oxide traps provides way to Fermi level pinning, in this circumstance interfacial layer need passivation (H_2 , S etc) to control Fermi level pinning. On the contrary for VDS-devices, passivation need not required at 300K as the frequency increase smoothly by decrease into inversion capacitance by increases in time constant (T). InSb VDS-MOS frequency dispersion in the accumulation region is alike to high- k oxides on InSb, which is attributed to Sb-O or In-O negligible inhomogeneous layer. Besides InSb VDS-substrate surface unpassivated (dangling bonds), and the defect generated during growth and oxidation processing could be suppressed. The traps distribution in the InSb band gap influence a Fermi level pinning, the electrically-active interface states by Sb and In, are significantly removed. InSb VDS-devices (p-n junction diode, Schottky diode, MOS structure) were from unpublished research of thesis [22].

V. Conclusion

On the potentiality and prospects of the detached crystals grown by VDS on earth the conclusions are - VDS-devices can maintain a stable ideality factor for high SBH on Sb-based substrates by reason of the high crystallinity. For the first time, SBD I-V, R_s plots showed lowest leakage (dark current), and an excellent rectifying junction at 300K. In addition, InSb VDS-MOS structure has been successfully developed, and characterized by I-V, C-V, C-F, $G(W)/W-F$ and low-frequency ideal C-V response, these showed an excellent result at 300K. Analysis of the conductance measurements in the strong inversion region indicates bulk generation, and dominates minority carrier by the thermal generation leading to excellent MOS structures. The interface layer is homogeneous and continuously distributed over the entire InSb band-gap. Also examined the effect of high quality InSb VDS-substrate, and excellent electrical characteristics of VDS-devices have presented. These device results show effective high-quality interface, and compared with the traditional devices. However, Sb-based detached crystals by VDS have high quality substrates, and potential application in third generation infrared (IR), and integrated circuit (IC) device.

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single crystal growth a new growth process by the detached phenomenon (concept) using vertical directional solidification (VDS) has been developed successfully for Sb-based (III-V) highest quality bulk crystals in a terrestrial lab (on Earth), while these crystals are analogous to the crystal grown in a microgravity. Dr. Gadkari was also member of professional International and National research journals. He has successfully completed Research projects (nine) sponsored by government of India and parent institute (SVKM). Indian patents on his name for the detached crystal growth by VDS in the terrestrial lab. This approach has opened a new area for high quality entire detached single crystal growth. He has received several kinds of awards/medals/certificates from academic societies such as Materials Chemistry and Physics, Indian Association of Crystal Growth, ASM International India Chapter, Shivaji University Kolhapur India, and several Research Institutes / Colleges within India and abroad.

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